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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,976	10/21/2003	Glenn A. Rinne	9180-24	3798

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,976	RINNE, GLENN A.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,7,9-19,21-27,29-31,33-40,42-52,55-57 and 63-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7,9-19,21-27,29-31,33-40,42-52,55-57 and 63-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-7, 9-19, 21-27, 29-31, 33-40, 42-52, 55, 57 and 63-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (6731009), hereinafter Jones in view of Bertin et al. (5977640), hereinafter Bertin and Perino et al. (6621155), hereinafter Perino.

Regarding claims 1, 9, 15, 19, 21-22, 29, 36, 42, 45-48, 50-52, 62, 64-65, 67-72, 74-77 and 79, Fig. 3C of Jones shows 1. (currently amended) An electronic device comprising:

a first integrated circuit substrate 308-0 with bumps;

a second integrated circuit electronic substrate 308-1 with bumps on the first integrated circuit electronic substrate;

a third integrated circuit electronic substrate 308-2 with bumps on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit electronic substrates;

circuit board 302 with bumps; and

the device sides of the first, second, and third integrated circuit substrates face a first direction, and the backsides of the first, second, and third integrated circuit substrates face a second direction.

Fig. 3C of Jones shows most aspect of the instant invention except a first electrical and mechanical connection between the first and third integrated circuit substrates wherein the first electrical bypasses the second integrated circuit substrate; a second electrical connection between the second and third integrated circuit electronic substrates; and a third electrical between the first and second integrated circuit substrates. Fig. 16 of Bertin shows an electrical connection (bumps) between the first and the third IC's 40, 40A bypassing the second IC and the second IC 30, 30A electrically connected to the first and the third. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jones with Bertin by an electrical connection between the first and the third bypassing the second and the second IC electrically connected to the first and the third for compact package.

The combination of Jones/Bertin fails to show a mechanical connection between the IC's. Fig. 3D of Perino shows a mechanical connection (495's; interposer) between the three IC's and all the IC's have the same size. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jones/Bertin with Perino by a mechanical connection and the same size of the IC' to secure the package and the same size of the IC's

Note that the combination of Jones/Bertin/Perino shows all the aspect regarding the first, second and third IC's and Fig. 3D of Perino shows a connection between the multiple layers of IC's. In addition, Fig. 3D of Perino shows an electrical connection between the IC's and the top IC's and the first bottom IC are connected to the signal via in the circuit board. Therefore, the combination of Jones/Bertin/Perino shows a direct electrical coupling between the IC's.

Regarding claims 2, 23, 43-44 and 73, 78, Fig. 3C of Jones shows wherein the second integrated circuit electronic substrate is offset relative to the first and third integrated circuit

substrates so that the first and third integrated circuit substrates (and the bumps) extend beyond an end of the second integrated circuit substrate.

Regarding claims 2-3 and 37 and 65-66, the combination of Jones/ Bertin/Perino would show the first electrical and mechanical connection (bumps) is spaced apart and between portions of the first and third integrated circuit substrates extending beyond the end of the second integrated circuit substrate.

Regarding claims 4, 6-7, 24-25 and 78, Fig. 16 of Bertin shows a conductive trace (bumps) on a surface of the first integrated circuit electronic substrate, the conductive trace providing an electrical coupling between the first and third electrical and mechanical connections and the first conductive bump is spaced apart from and extends past an edge of the second integrated circuit substrate, and wherein the second electrical and mechanical connection comprises a second conductive bump between the second and third integrated circuit electronic substrates. Note that it is obvious that there are conductive traces on the surface of the IC's since the bumps are connected to the surface.

Regarding claims 10-13, 30, 33 and 49, Perino discloses a memory device (col. 1, lines 9-13), therefore, bumps of Bertin would be coupled to I/O's of data and address.

Regarding claim 14, Fig. 16 of Bertin shows the first and third integrated circuit electronic substrates comprise memory devices having a same layout.

Regarding claims 16 and 31, the combination of Jones/ Bertin/Perino would show the printed circuit board includes a first conductive pad to which the third electrical and a conductive bump is bonded and a second conductive pad to which the fourth is boned wherein the first

conductive pad has a greater surface area than the second conductive pad and the bumps give mechanical connection since they connect the IC's.

Regarding claims 17, 38 and 40, the combination of Jones/ Bertin/Perino would show a first conductive trace on the printed circuit board providing electrical coupling between the third and fourth bupms a second conductive trace on the second integrated circuit substrate providing electrical coupling between the fourth and fifth conductive bumps; and a third conductive trace on the first substrate providing electrical coupling between the fifth and first conductive bumps.

Regarding claim 18, subject matter ahs been discussed in claims 9-12.

Regarding claims 27 and 34, the combination of Jones/ Bertin/Perino would show all the aspect of the instant invention as discussed in claim 1 and Fig. 3D of Perino shows that all the IC's have the same size.

Regarding claim 28, Fig. 16 of Bertin shows the first conductive bump has a greater volume than the second conductive bump.

Regarding claim 55, Fig. 3D of Perino shows an electrical connection without bumps.

Regarding claims 57 and 59, Fig. 16 of Bertin shows the bumps in the first and third IC's are in mirror image.

Regarding claim 58, Fig. 16 of Bertin shows some of the bumps are in an array on a one to one basis.

Regarding claim 60, subject matter ahs been discussed in claims 9-12.

Regarding claim 63, Fig. 3D of Perino shows that back of the board without an IC.

Claim 56 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jones/ Bertin/Perino as applied to claim 55 above, and further in view of Shangguan et al. (6082610), hereinafter Shangguan.

Regarding claim 56, the combination of Jones/ Bertin/Perino would show all the aspect of the instant invention except the solder bump with a wettable pad. Shangguan discloses the solder bump with a wettable pad (col. 1, lines 55-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jones/Bertin/Perino with Shangguan by having the solder bump with a wettable pad for easy bump connection.

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Douglas W. Owens 11/25/06

jmi

DOUGLAS W. OWENS
PRIMARY EXAMINER